**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (CANCELLED)
2. (CANCELLED)
3. (CANCELLED)
4. (CANCELLED)
5. (CANCELLED)
6. (CANCELLED)
7. (CANCELLED)
8. (CANCELLED)
9. (CANCELLED)
10. (CANCELLED)
11. (CANCELLED)
12. (CANCELLED)
13. (CANCELLED)
14. (CANCELLED)
15. (CANCELLED)
16. (CANCELLED)
17. (CANCELLED)
18. (CANCELLED)
19. (CANCELLED)
20. (CANCELLED)
21. (CANCELLED)
22. (CANCELLED)
23. (CANCELLED)

24. (Currently Amended) The amplifier according to claim ~~23~~25, wherein said DC signal is a DC current for said first transistor.

25. (Currently Amended) An amplifier comprising:

a first and a second interconnected transistor;

an associated dynamic biasing circuit comprising:

means for generating a dynamic bias signal based on detection of a direct current, DC, signal of said first transistor; and

means for applying said dynamic bias signal to said second transistor;~~The amplifier according to claim 23,~~

~~wherein~~ said first transistor having an input electrode adapted for receiving an input signal and an output electrode connected to an input terminal of said dynamic biasing circuit and to an input electrode of said second transistor, said dynamic biasing circuit having an output terminal connected to said input electrode of said second transistor, and said second transistor having an output electrode adapted for providing an output signal.

26. (Currently Amended) An amplifier comprising:

a first and a second interconnected transistor;

an associated dynamic biasing circuit comprising:

means for generating a dynamic bias signal based on detection of a direct current, DC, signal of said first transistor; and

means for applying said dynamic bias signal to said second transistor;~~The amplifier according to claim 23,~~

wherein an input electrode of said first transistor and of said second transistor is adapted for receiving an input signal and an output electrode of said first transistor and of said second transistor is adapted for providing an output signal, said dynamic biasing circuit having an input terminal connected to said output electrode of said first transistor and an

output terminal distinct from the input terminal connected to ~~said~~ a base ~~input~~ electrode of said second transistor.

27. (Cancelled)

28. (Currently Amended) An amplifier comprising:

a first and a second interconnected transistor;

an associated dynamic biasing circuit comprising:

means for generating a dynamic bias signal based on detection of a direct current, DC, signal of said first transistor; and

means for applying said dynamic bias signal to said second transistor, said bias signal generating means being arranged for detecting a voltage drop caused by said DC signal and for generating said dynamic bias signal based on said detected voltage drop;

~~The amplifier according to claim 27, wherein~~ said dynamic biasing circuit comprising~~comprises~~:

- resistance means connected to an output electrode of said first transistor and arranged for connection with a supply voltage;
- and an operation amplifier having a first input terminal connected to said output electrode of said first transistor, a second input terminal for connection with said first supply voltage and an output terminal connected to an input electrode of said second transistor, said operational amplifier ~~is~~ being adapted for detecting said voltage drop as a difference between a first input voltage of said first input terminal and a second input voltage of said second input terminal.

29. (Previously Presented) The amplifier according to claim 28, wherein said operational amplifier is adapted for generating an output voltage signal proportional to said detected voltage drop, said dynamic bias signal comprising said output voltage signal.

30. (Currently Amended) The amplifier according to claim ~~27~~25, wherein said dynamic biasing circuit comprises:

- resistance means connected to an output electrode of said first transistor and arranged for connection with a supply voltage;
- and a third transistor having an input terminal arranged for connection with said supply voltage and an output electrode connected to said output electrode of said first transistor and to an input electrode of said second transistor, said third transistor detecting said voltage drop as a difference between a first input voltage of said input electrode and a second input voltage of said output electrode.

31. (Currently Amended) The amplifier according to claim ~~23~~25, further comprising a fourth transistor connected to said applying means and adapted for adjusting said dynamic bias signal for said second transistor.

32. (Cancelled)

33. (Currently Amended) An amplifier comprising:

a first and a second interconnected transistor;

an associated dynamic biasing circuit comprising:

means for generating a dynamic bias signal based on detection of a direct current, DC, signal of said first transistor;

means for applying said dynamic bias signal to said second transistor, said bias signal generating means being arranged for detecting a voltage drop caused by said DC signal and for generating said dynamic bias signal based on said detected voltage drop;

~~The amplifier according to claim 32, further comprising:~~

a fifth transistor cascade connected to said first transistor, said applying means is configured for applying said dynamic bias signal to said fifth transistor;

[[-]] a first voltage dividing circuit having an input terminal connected to said applying means and an output terminal connected to said second transistor; and

[[-]] a second voltage dividing circuit having an input terminal connected to said applying means and an output terminal connected to said fifth transistor.

34. (Cancelled)

35. (Currently Amended) The circuit according to claim ~~34~~37, wherein said DC signal is a DC current for said first transistor.

36. (Cancelled)

37. (Currently Amended) A dynamic biasing circuit for biasing an amplifier comprising a first transistor and a second interconnected transistor, said circuit comprising:

- means for generating a dynamic bias signal based on detection of a direct current, DC, signal of said first transistor; and
- means for applying said dynamic bias signal to said second transistor; ~~The circuit according to claim 36,~~

wherein bias signal generating means is arranged for detecting a voltage drop caused by said DC signal and for generating said dynamic bias signal based on said detected voltage drop , and wherein said dynamic biasing circuit comprises:

- resistance means connected to an output electrode of said first transistor and arranged for connection with a supply voltage; and
- an operation amplifier having a first input terminal connected to said output electrode of said first transistor, a second input terminal for connection with said first supply voltage and an output terminal connected to an input electrode of said second transistor, said operational amplifier detecting said voltage drop as a difference between a first input voltage of said first input terminal and a second input voltage of said second input terminal.

38. (Previously Presented) The circuit according to claim 37, wherein said operational amplifier is adapted for generating an output voltage signal proportional to said detected voltage drop, said dynamic bias signal comprising said output voltage signal.

39. (Currently Amended) The circuit according to claim ~~36~~37, wherein said dynamic biasing circuit comprises:

- resistance means connected to an output electrode of said first transistor and arranged for connection with a supply voltage; and
- a third transistor having an input terminal arranged for connection with said supply voltage and an output electrode connected to said output electrode of said first transistor and to an input electrode of said second transistor, said third transistor detecting said voltage drop as a difference between a first input voltage of said input electrode and a second input voltage of said output electrode.

40. (Currently Amended) The circuit according to claim ~~34~~37, further comprising a fourth transistor connected to said applying means and adapted for adjusting said dynamic bias signal for said dynamically biasing circuit.

41. (Currently Amended) A method for dynamically biasing an amplifier comprising a first transistor and a second interconnected transistor, the method comprises:

applying an input signal to an input electrode of said first transistor and to an input electrode of the second transistor~~, said method comprising the steps of:~~;

[[-]] applying a direct current signal of the first transistor to an input electrode of said second transistor and to an input terminal of a dynamic biasing circuit;

generating with the dynamic biasing circuit ~~generating~~ a dynamic bias signal based on detection of a the direct current~~, DC,~~ signal of said first transistor; and

[[-]] applying said dynamic bias voltage signal to the input electrode of said second transistor;

outputting an amplified signal from an output electrode of the second transistor.

42. (Currently Amended) The method according to claim 41, wherein said direct current ~~DC~~ signal is a direct current ~~DC~~ current for said first transistor.

43. (Currently Amended) The method according to claim 41, wherein generating said bias signal ~~generating step~~ comprises ~~the steps of~~:

- applying said ~~DC~~ direct current signal to at least one resistance ~~means~~;
- detecting a voltage drop over said resistance ~~means~~ caused by said ~~DC~~ direct current signal; and
- generating a voltage signal proportional to said detected voltage drop, said dynamic bias signal comprises said generated voltage signal.

44. (Currently Amended) The method according to claim 41, wherein generating said bias signal ~~generating step~~ comprises adjusting said dynamic bias signal for said second transistor.

45. (New) An amplifier comprising:

a first and a second interconnected transistor;

an associated dynamic biasing circuit comprising a dynamic bias signal generator configured to generate a bias signal for application to the second transistor based on detection of a direct current signal of said first transistor; and

said first transistor having an input electrode adapted for receiving an input signal and an output electrode connected to an input terminal of said dynamic biasing circuit and to an input electrode of said second transistor, said dynamic biasing circuit having an output terminal connected to said input electrode of said second transistor, and said second transistor having an output electrode adapted for providing an output signal.

46. (New) An amplifier comprising:

a first and a second interconnected transistor;

an associated dynamic biasing circuit comprising a dynamic bias signal generator configured to generate a bias signal for application to the second transistor based on detection of a direct current signal of said first transistor;

wherein an input electrode of said first transistor and of said second transistor is adapted for receiving an input signal and an output electrode of said first transistor and of said second transistor is adapted for providing an output signal, said dynamic biasing circuit having an input terminal connected to said output electrode of said first transistor and an output terminal distinct from the input terminal connected to a base electrode of said second transistor.

47. (New) An amplifier comprising:

a first and a second interconnected transistor;

an associated dynamic biasing circuit comprising a dynamic bias signal generator configured to generate a bias signal for application to the second transistor based on detection of a direct current signal of said first transistor, said bias signal generator being arranged for detecting a voltage drop caused by said DC signal and for generating said dynamic bias signal based on said detected voltage drop;

said dynamic biasing circuit comprising:

- at least one resistor connected to an output electrode of said first transistor and arranged for connection with a supply voltage;
- and an operation amplifier having a first input terminal connected to said output electrode of said first transistor, a second input terminal for connection with said first supply voltage and an output terminal connected to an input electrode of said second transistor, said operational amplifier being adapted for detecting said voltage drop as a difference between a first input voltage of said first input terminal and a second input voltage of said second input terminal.